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WHITE PAPER

Scalable, Cloud-Ready IC Validator Solution for Advanced DRC Nodes

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Introduction

As we move to a data-centric world, semiconductor companies across the globe are working at a furious pace to develop and manufacture Artificial Intelligent [AI] chips. AI is all about an algorithm that mimics a human's ability to learn and decide. For example, AI can be used to interpret and understand an image that helps a doctor make a better diagnosis for a patient. This requires chips to handle massive amounts of mathematical computations to find patterns and make inferences. Hence, AI chips pack a tremendous amount of computing power that provides the ability to quickly process large amounts of data. The requirement to add more functionality on a chip drives chip designers to move to the cutting edge of process technology. This in turn increases the physical verification complexity.

Physical Verification Trends and Challenges

As you move to deep sub-micron technology nodes, physical verification steps must deal with numerous rules with increased complexity. For example, in the 16/20nm technology DPT (Double Patterning), checks are introduced that cause the runset to have numerous DRC rules and DRC runset operations. Figure 1 shows the design size graph for every technology node and Figure 2 shows DRC rules and the number of DRC operations per node in the runset. The very latest technology node includes triple patterning and quadruple/multiple patterning as well. At 7nm, the runset can have up to 10,000 rules. Most of these rules are very complex, therefore close to 100K DRC computational operations are required to implement these rules in the runset.

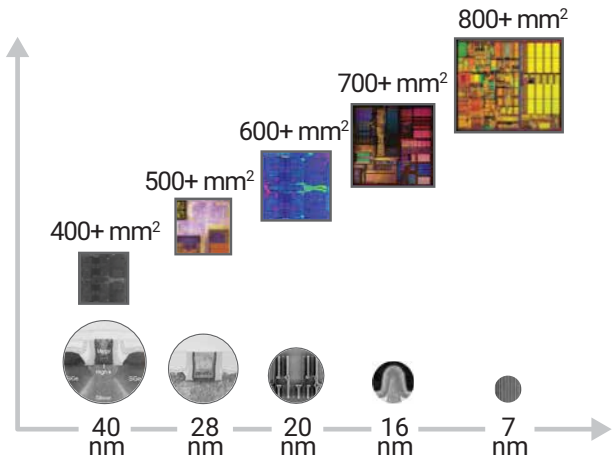

Figure 1: Big and complex designs

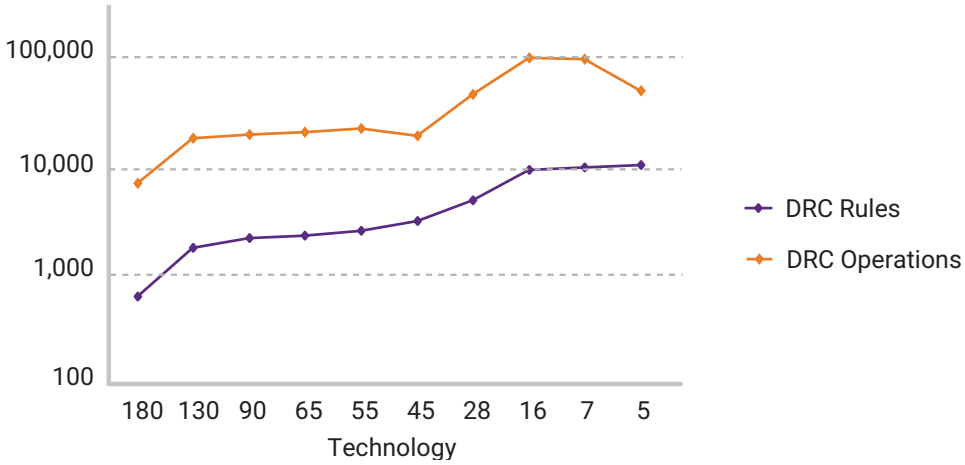

Figure 2: Increasing DRC complixity

While the number of rules does not increase at the 5nm node due to EUV (Extreme Ultraviolet) lithography technology, they still add complexity with requirements such as the following:

I. All poly (including dummy poly) must be on a poly-grid
II. Vias are grouped by critical pitch. Via space constraints are different
III. MEOL (Middle End Of Line) metals can be only 1-D (rectangle)
IV. More numbers of “empty area”, “max space” checks

These requirements contribute to more complex rules in the DRM (Design Rule Manual), and these complex rules are implemented with many DRC operations in the runset. The IC Validator team works closely with foundry partners to understand these requirements early in the manufacturing process development cycle. This early engagement helps the IC Validator team develop macro-level functions in the PXL language to implement complex rules in the runset for deep sub-micron technologies.

Design size, the number of DRC rules, and the complexity of the rules increase heavily node by node, which means it takes a long time to complete a DRC step. But, the customer requirement on DRC runtime does not change. Customers want to complete their physical verification runs overnight.

Methods for Getting Faster DRC Performance

There are several ways to achieve a faster DRC runtime. For example,

- Split rule decks and have multiple, different sets of DRC runs
- Run fewer numbers of rules or only a portion of the runset
- Increase CPU power, additional hardware resources

These methods have their pros and cons. Manually splitting the deck requires experience with rule-deck development, or running with switches in the rule deck might result in missing rules. And, running with fewer numbers of rules or a portion of the runset still might miss some rules or increase the number of iterations to complete the DRC job. By running with more powerful and newly threaded architecture machines without touching the rule deck, it is possible to achieve accurate DRC results in few hours without compromising anything. The hardware resources are available and customers are asking EDA vendors to utilize this hardware intelligently to achieve faster time-to-tapeout.

The IC Validator Scalable and Cloud-Ready Solution

EDA tools must utilize a massive number of machines and the new threading architecture to provide faster performance. The IC Validator engine has a unique distributed processing and multi-threading capability, which runs the DRC rules deck with any number of cores/CPUs. The IC Validator scalability is out of the box and very easy to use. Figure 3 shows IC Validator scalability results with up to 1000 cores running on a 7nm test chip design. With real production, larger design, we expect to see even better scaling since there are more opportunities to parallelize more commands. With 200 cores, it achieves the customer's overnight [8hrs] runtime requirements. With 500 cores, the runtime is less than 4hrs, which allows the customer to run full-chip DRC a few times a day. By adding more cores, you can still reduce the runtime; in this case, by adding 1000 cores, the runtime is less than 3 hours Highly powerful machines and the IC Validator tool's unique distributed processing and multi-threading capability enables the customer to get full-chip results in just few hours without modifying the runset.

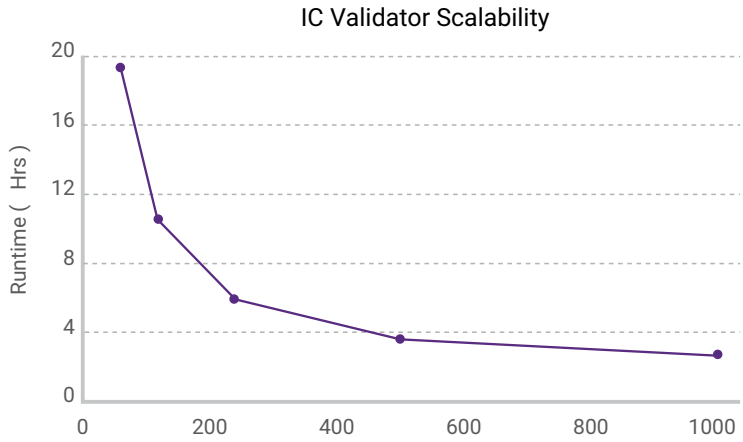

Figure 3: Scalability results with 1000 Cores

How do you obtain the number of cores needed to complete a full-chip design? EDA tools should be able to run on the cloud, whether private or public, to access an unlimited number of cores to achieve faster runtime and performance. Figure 4 and Figure 5 show the IC Validator use model with the cloud. One use model is to keep the design, license, hardware resources, and EDA tool binaries in the cloud to perform an operation. This is mostly possible with a private cloud. The other use model is to keep the design, license, and EDA tool binaries outside of the cloud and access only the hardware resources in the cloud. IC Validator distributed processing combined with multi-threading architecture works well with low-cost smaller capacity machines, therefore providing the ability to use more cores to achieve faster results. Ultimately, cloud-ready tools must work within the smaller memory limits of public clouds for optimal efficiency. IC Validator scalable architecture makes full use of the smaller memory machines to deliver the fastest possible performance using the flexible compute environment of the cloud. The IC Validator tool is successfully used in the cloud when taping out a customer's large SoC advanced node designs.

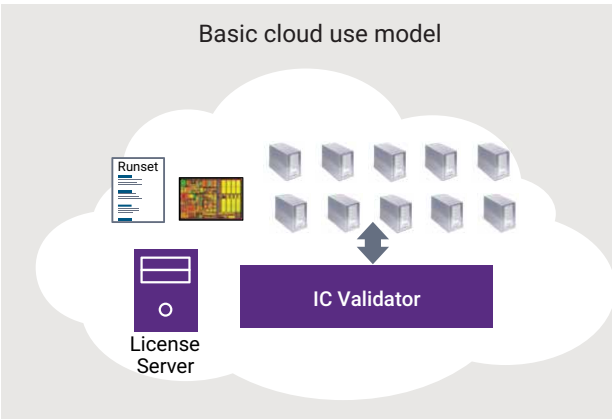

Figure 4: Basic cloud use model

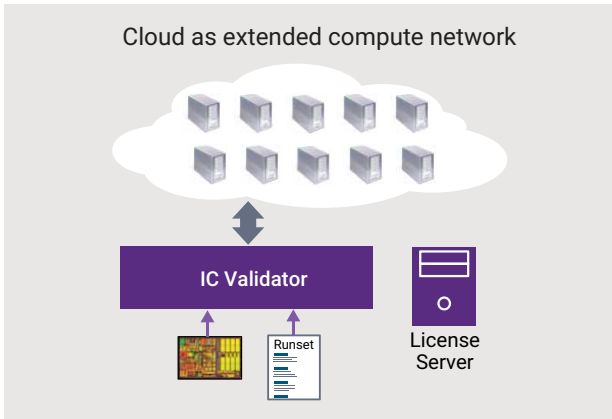

Figure 5: Cloud as extended compute network

Conclusion

The scalable and cloud-ready architecture of the IC Validator tool enables you to achieve DRC results for extremely large designs in just a few hours. If you make designs in very deep sub-micron technologies, you can confidently use the IC Validator tool to tape out your large designs. With the IC Validator tool, the physical verification step will not be in your critical path!

For more information, please go to synopsys.com/icvalidator

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